IN THE CLAIMS

Please amend and consider the claims as follows:

1. (Currently Amended) An integrated circuit having a top metal layer, the top metal layer having a first metal bar and a second metal bar, the integrated circuit comprising:

a first bump disposed on the first metal bar;

a second bump disposed on the first metal bar, wherein the first bump is adjacent to the second bump; and

a reference bump disposed on the second metal bar,

wherein the first bump and the second bump are positioned such that an angle between a line from the reference bump to the first bump and a line from the reference bump to the second bump has a value substantially equal to 150 degrees.

2. (Previously Amended) The integrated circuit of claim 1, wherein the first bump, the second bump, and the reference bump form a bump structure that is repeated across the top metal layer to form a patterned bump array.

3. (Previously Amended) The integrated circuit of claim 1, wherein the first bump, the second bump, and the reference bump for a bump structure that is repeated across a portion of the top metal layer.

4. (Previously Amended) The integrated circuit of claim 1, wherein the first metal

bar is operatively connected to a voltage source, and wherein the second metal bar is operatively connected to ground.

5. (Previously Amended) The integrated circuit of claim 1, wherein the value of the angle is dependent on at least one selected from the group consisting of: a desired capacitance, a desired resistance, a desired inductance, a desired bump current flow, a desired bump population on the top metal layer, and desired signal track availability.

6. (Currently Amended) An integrated circuit having a top metal layer, the top metal layer having a first metal bar and a second metal bar, the integrated circuit comprising:

a first bump disposed on the first metal bar;

a second bump disposed on the first metal bar, wherein the first bump is adjacent to the second bump; and

a reference bump disposed on the second metal bar,

wherein the first metal bar and the second metal bar are positioned such that an angle between a line from the reference bump to the first bump and a line from the reference bump to the second bump has a value substantially equal to 150 degrees.

7. (Previously Amended) The integrated circuit of claim 6, wherein the first bump, the second bump, and the reference bump form a bump structure that is repeated

across the top metal layer to form a patterned bump array.

8. (Previously Amended) The integrated circuit of claim 6, wherein the first bump, the second bump, and the reference bump for a bump structure that is repeated across a portion of the top metal layer.

9. (Previously Amended) The integrated circuit of claim 6, wherein the first metal bar is operatively connected to a voltage source, and wherein the second metal bar is operatively connected to ground.

10. (Previously Amended) The integrated circuit of claim 6, wherein the value of the angle is dependent on at least one selected from the group consisting of: a desired capacitance, a desired resistance, a desired inductance, a desired bump current flow, a desired bump population on the top metal layer, and desired signal track availability.

11. (Currently Amended) A patterned bump array for a power grid of an integrated circuit, comprising:

a reference bump disposed on a first metal bar;

a first bump disposed on a second metal bar; and

a second bump disposed on a second metal bar,

wherein the first bump is adjacent to the second bump, and

wherein the first bump, the second bump, and the reference bump are

arranged such that an angle between a line from the reference bump to the first bump and a line from the reference bump to the second bump has a value substantially equal to 150 degrees.

12. (Previously Amended) The patterned bump array of claim 11, wherein the first metal bar and second metal bar form a portion of the power grid.

13. (Previously Amended) The patterned bump array of claim 11, wherein the first metal bar is operatively connected to power, and wherein the second metal bar is operatively connected to ground.

14. (Previously Amended) The patterned bump array of claim 11, wherein the arrangement of the first bump, the second bump, and the reference bump is repeated across the power grid.

15. (Previously Amended) The patterned bump array of claim 11, wherein the arrangement of the first bump, the second bump, and the reference bump is repeated across a portion of the power grid.

16. (Previously Amended) The patterned bump array of claim 11, wherein the value of the angle is dependent on at least one selected from the group consisting of: a desired capacitance, a desired resistance, a desired inductance, a desired bump

current flow, a desired bump population on the top metal layer, and desired signal track availability.

17. (Currently Amended) A bump layout for a power grid of an integrated circuit, comprising:

a reference bump disposed on a first metal bar;

a first bump disposed on a second metal bar; and

a second bump disposed on a second metal bar,

wherein the first bump is adjacent to the second bump, and

wherein the first metal bar and the second metal bar are arranged such that an angle between a line from the reference bump to the first bump and a line from the reference bump to the second bump has a value substantially equal to 150 degrees.

18. (Previously Amended) The bump layout of claim 17, wherein the first metal bar and second metal bar form a portion of the power grid.

19. (Previously Amended) The bump layout of claim 17, wherein the first metal bar is operatively connected to power, and wherein the second metal bar is operatively connected to ground.

20. (Previously Amended) The bump layout of claim 17, wherein the arrangement of the first metal bar and the second metal bar is repeated across the power grid.

21. (Previously Amended) The bump layout of claim 17, wherein the arrangement of the first metal bar and the second metal bar is repeated across a portion of the power grid.

22. (Previously Amended) The bump layout of claim 17, wherein the value of the angle is dependent on at least one selected from the group consisting of: a desired capacitance, a desired resistance, a desired inductance, a desired bump current flow, a desired bump population on the top metal layer, and desired signal track availability.

23. (New) The integrated circuit of claim 1, wherein the first metal bar and the second metal bar are substantially interlocked.

24. (New) The integrated circuit of claim 23, wherein there is a finite amount of spacing between the first metal bar and the second metal bar.

25. (New) The integrated circuit of claim 1, wherein the first bump, the second bump, and the reference bump are partially aligned.